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EXAMINER

DOAN, DUC T

ART UNIT

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NOTIFICATION DATE

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ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/008,872	Applicant(s) LIN ET AL.	
	Examiner DUC T. DOAN	Art Unit 2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period **will** apply and **will** expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply **will**, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 28 July 2010.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 3,5,6,11-17 and 20-23 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 3, 5-6, 11-17 and 20-23 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Status of Claims

Claim 23 have been added.

Claims 1-2, 4, 8-10 and 18-19 have been canceled.

Claims 3, 5-6, 11-17 and 20-23 remain pending.

Claims 3, 5-6, 11-17 and 20-23 are rejected.

Applicant's remarks filed 7/28/2010 have been fully considered but they are mooted in view of new ground(s) of rejection necessitated by the Applicant's amendments to the claims.

Claims Objections

Claims 11-16, 23, 3, 5-6 are objected because of the following informalities:

As in claim 11, line 2-3, "the address for data the data block" lacks antecedent basis. And it not clear whether it referred to the address of data block recited in claim 7.

Claims 12 line 2, "the command block address" lacks antecedent basis.

As in claim 13, line 2, "the data block address" lack antecedent basis and it not clear whether it referred to the address of data block recited in claim 7.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

As in claim 23,

Line 6, "receive the digital signals" lacks antecedent basis and not clear. Digital signals have not been claimed and/or described where they are received from.

line 22, "the digital signal" is not clear. It is unclear whether it intends to refer to the digital signals at line 6 or the digital signal at line 19.

U.S.C. 112, second paragraph

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 23, 3, 5-7, 11-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As in claim 7, line 8, "setting an indicator signal in a defined memory location" is not clear. Defined memory is not defined nor has it been previously recited.

As in claim 23,

line 26, "... to provide the transmitter circuitry" is not clear. The term "the transmitter circuitry" lacks antecedent basis, and it is not clear whether it intends to refer to something is to provide for the "transmission circuitry" recited in claim 4, or intends to furnish a function "transmitter circuitry".

All dependent claim(s) are rejected as having the same deficiencies as the claim(s) they depend from.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 23, 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mohebbi et al (US Pub. 2003/0108119) in view of Auckland et al (US Pub. 2002/0183013) and in further view of Hudgins Jr. (US pat. 4615001, herein Hudgins) and Micalizzi Jr. et al (US Pat. 6434630, herein Micalizzi).

As in claim 23, Mohebbi discloses a wireless transceiver device, comprising: baseband processing circuitry coupled to provide the digital signals to the transmission circuitry and to receive the demodulated digital signals from the receiver circuitry (par. 2-3, 30 Fig 5, base band processing circuit 200 for processing wireless information).

Mohebbi does not disclose the claim's details related to frequency conversion. However, Auckland discloses

a transmit/receive switch to selectively transmit radio frequency signals and to receive radio frequency signals (par. 77-78 and 92 Fig 6 switch for transmitting and receiving frequency signals);

transmission circuitry to receive digital data and to convert the digital data to radio frequency signals for transmission, the transmission circuitry includes:

modulation circuitry coupled to receive the digital signals and produce modulated digital signals (par. 88, Fig 6 616 modulation); digital-to-analog conversion circuitry coupled to convert the modulated digital signals to converted analog signals88, (Fig 6 616 A/D);

up-converter coupled to receive to convert the modulated digital signals to produce outgoing radio frequency signals for transmission via the transmit/receive switch (par. 88, Fig 6 616 up converter);

receiver circuitry coupled to receive radio frequency signals from the transmit/receive switch (Fig 6, 610 received RF from antenna), the receiver circuitry includes:

down-converter coupled to receive the radio frequency signals from the transmit/receive switch and produce down-converted radio signals (par. 88, Fig 6 610 down converter);

analog-to-digital conversion circuitry coupled to convert the down- converted radio signals to digital signals (par. 88, Fig 6 610 A/D); and

demodulation circuitry coupled to receive the digital signals from the analog-to-digital conversion circuitry and produce demodulated digital signals (par. 88, Fig 6);

It would have been obvious to one of ordinary skill in the art at the time of invention to include configurable front end as suggested by Auckland in Mohebbi's system to transmit and receive signals efficiently and thereby further improve the performance of the overall system (par. 48).

Mohebbi and Auckland do not disclose the claim's details memory structures of processing circuitry. However, Hudgins discloses

a first in, first out (FIFO) memory structure for storing addresses (col. 6, lines 40-48, message queue stores request which is represented by a pointer to the transaction request message; queue is implemented as circular queue, i.e. claim's FIFO, col. 4 lines 17-40);

for accessing data blocks to order the digital data to provide the transmitter circuitry (col. 6 line 63 to col. 7 line 7, a message in the queue has associating command and data for sending / receiving).

It would have been obvious to one of ordinary skill in the art at the time of invention to include message structure in memory as suggested by Huggins in Mohebbi's system modified by Auckland to transmit and receive signals efficiently and thereby further improve the performance of the overall system (par. 48).

Mohebbi, Auckland, Hudgins does not disclose the claim's command block includes address of data block. However, Micalizzi discloses

a plurality of command blocks formed within another memory structure and a portion of the another memory structure that stores an indicator that indicates whether a

command block of the plurality of command blocks is in use (Fig 3A, IOCB command control block 100 ; col. 12, lines 1-15, status information of I/O command);

wherein each of the command blocks includes addresses of data blocks stored within the another memory structure (Fig 3A, IOCB command control block 100 with data segment addresses for data blocks).

It would have been obvious to one of ordinary skill in the art at the time of invention to include addresses of data blocks as suggested by Micalizzi in Mohebbi's system modified by Auckland, Hudgins thus segments of data can be retrieved and processed efficiently and thereby further improve the performance of the overall system (col. 8 lines 35-47),

As in claim 3, Mohebbi and Auckland do not disclose the claim's pointer. However, Hudgins discloses wherein the FIFO memory structure includes pointers that define addresses of the command blocks (col. 6, lines 40-48, message queue stores request which is represented by a pointer to the transaction request message). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt the teaching of Hudgins in Mohebbi's system modified by Auckland for the same reasons stated above.

As in claim 5, Mohebbi does not disclose the claim's Gaussian Phase Shift Keying. However, Auckland discloses wherein the modulation circuitry includes Gaussian Phase Shift Keying modulation and the demodulation circuitry includes Gaussian Phase Shift Keying demodulation circuitry (Auckland's par. 147, lines 2-4)

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mohebbi et al (US Pub. 2003/0108119) in view of Auckland et al (US Pub. 2002/0183013) and in further view of Hudgins Jr. (US pat. 4615001, herein Hudgins) and Micalizzi Jr. et al (US Pat. 6434630, herein Micalizzi) and Shi et al (US Pub. 2002/0199210).

As in claim 6, Mohebbi, Auckland, Hudgins and Micalizzi do not disclose the claim's baseband frequency. However, Si discloses wherein each of the up-converter and the down-converter converts directly between radio frequency and baseband frequency (up/down convert directly into baseband frequency). It would have been obvious to one of ordinary skill in the art at the time of invention to include bandwidth selector as suggested by Si in Mohebbi's system modified by Auckland, Hudgins and Micalizzi thus appropriate frequency range can be selected effectively and thereby further improve the overall performance of the system.

Claims 7, 11-17, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mohebbi et al (US Pub. 2003/0108119) in view of Hudgins Jr. (US pat. 4615001, herein Hudgins) and in further view and Micalizzi Jr. et al (US Pat. 6434630, herein Micalizzi).

As in claim 7, Mohebbi discloses a method for storing and accessing data in a baseband processing circuitry for transmission by a wireless communication device (par. 2-3, 30 Fig 5, base band processing circuit 200 for processing wireless information), comprising: storing a data block in random access memory of the

baseband processing circuitry (par. 8 and 11, FB and RC as memory for storing data / instructions accessed by processor, which typical is a random access memory);

Mohebbi does not disclose the claim's details memory structures of processing circuitry. However, Hudgins discloses

storing a pointer that corresponds to the data block in a first in, first out (FIFO) memory structure of the baseband processing circuitry, the pointer includes an address of a command block (col. 6, lines 40-48, message queue stores request which is represented by a pointer to the transaction request message; queue is implemented as circular queue, i.e. claim's FIFO, col. 4 lines 17-40),

It would have been obvious to one of ordinary skill in the art at the time of invention to include message structure in memory as suggested by Huggins in Mohebbi's system to transmit and receive signals efficiently and thereby further improve the performance of the overall system (par. 48).

Mohebbi and Hudgins do not discloses the claim's address of data block stored in command block. However, Micalizzi discloses storing an address of the data block in the command block (Fig 3A, IOCB command control block 100 with data segment addresses for data blocks);

and setting an indicator signal in a defined memory location, wherein the indicator signal indicates that the data block address stored in the command block is for data that has yet to be successfully transmitted by the wireless communication device and that the command block is busy (col. 12, lines 1-15, status information of I/O command).

It would have been obvious to one of ordinary skill in the art at the time of invention to include addresses of data blocks as suggested by Micalizzi in Mohebbi's system modified by Hudgins thus segments of data can be retrieved and processed efficiently and thereby further improve the performance of the overall system (col. 8 lines 35-47),

As in claim 11, Mohebbi and Hudgins do not disclose the claim's address of data block stored in command block. However, Micalizzi discloses wherein the address for the data block is only stored in a command block if the indicator signal reflects that the command block does not contain the address of a data block that has yet to be successfully transmitted (col. 7 lines 1-10, col. 8 lines 1-20, IOCB stores addresses of data segments for the I/O command to be processed). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt the teaching of Micalizzi in Mohebbi's system modified by Hudgins for the same reasons stated above.

As in claim 12, Mohebbi does not expressly disclose the claim's command block address. However, Hudgins discloses evaluating the command block address included within the FIFO pointer (col. 6, lines 40-48, message queue having request which is represented by a pointer to the transaction request message). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt the teaching of Hudgins in Mohebbi's system for the same reasons stated above.

As in claim 13, Mohebbi and Hudgins do not disclose the claim's data block address. However, Micalizzi discloses examining the contents of the command block specified by the pointer to determine the data block address (Fig 3A, IOCB command

control block 100 with data segment address for data block). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt the teaching of Micalizzi in Mohebbi's system modified by Hudgins for the same reasons stated above.

As in claim 14, Mohebbi and Hudgins do not disclose the claim's data block address. However, Micalizzi discloses evaluating at least a first memory location of the data block whose address is stored in the command block to determine a data block size (Fig 3A, IOCB command control block 100 with data segment addresses and data segment lengths for data blocks). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt the teaching of Micalizzi in Mohebbi's system modified by Hudgins for the same reasons stated above.

As in claim 15, Mohebbi and Hudgins do not disclose the claim's data block address. However, Micalizzi discloses retrieving an amount of data corresponding to the data block size and providing the data to a radio modem for transmission over wireless airwaves (Fig 3A, data segment length. Examiner note: Mohebbi already taught providing data over wireless radio, see par. 3). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt the teaching of Micalizzi in Mohebbi's system modified by Hudgins for the same reasons stated above.

As in claim 16, Mohebbi and Hudgins do not disclose the claim's indicator. However, Micalizzi discloses resetting the indicator signal when the transmission is successful (col. 12, lines 1-15, status information of I/O command for completion).

As in claim 17, Mohebbi discloses a memory structure formed within a baseband processing baseband processing circuitry (par. 2-3, 30 Fig 5, base band processing circuit 200 for processing radio wireless information), comprising:

a random access memory portion defined within the baseband processing circuitry to store data blocks that are to be transmitted via a radio modem (par. 8 and 11, FB and RC as memory for storing data / instructions accessed by processor, which typical is a random access memory).

Mohebbi does not disclose the claim's FIFO structure of the processing circuitry. However, Hudgins discloses

data in a first in, first out (FIFO) order (col. 6 line 65 to col. 7 line 7, data is referred by message queue in FIFO circular order, col. 4 lines 17-40);

a FIFO memory structure defined within the baseband processing circuitry to store pointers that correspond to the data blocks stored in the random access memory portion (col. 6, lines 40-48, message queue stores request which is represented by a pointer to the transaction request message; queue is implemented as circular queue, i.e. claim's FIFO, col. 4 lines 17-40).

Mohebbi and Hudgins do not discloses the claim's address of data block stored in command block specifying address of data block. However, Micalizzi discloses a plurality of command blocks further defined within the random access memory portion wherein each of the command blocks specifies an address of a data block that is to be transmitted (col. 8 lines 1-45, Fig 3A, IOCB, command control block 100 with data segment addresses for data blocks); and

a defined memory portion for that stores command block indicators for each command block, wherein the each of the command block indicators specify whether its corresponding command block includes the address of a data block that has yet to be successfully transmitted via the radio modem (col. 12, lines 1-15, status information of I/O command).

It would have been obvious to one of ordinary skill in the art at the time of invention to include addresses of data blocks as suggested by Micalizzi in Mohebbi's system modified by Hudgins thus segments of data can be retrieved and processed efficiently and thereby further improve the performance of the overall system (col. 8 lines 35-47).

As in claim 20, Mohebbi and Hudgins do not disclose the claim's indicator. However, Micalizzi discloses the defined memory portion that stores the command block indicators are each one bit in length (col. 13 lines 19-25, successful status). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt the teaching of Micalizzi in Mohebbi's system modified by Hudgins for the same reasons stated above.

As in claim 22, Mohebbi and Hudgins do not disclose the claim's corresponding to the data blocks. However, Micalizzi discloses wherein the FIFO memory structure defines a plurality of FIFO memory blocks in which each FIFO memory block correspond to the data blocks that are to be transmitted to a particular device (Fig 3A, IOCB command control block 100 corresponds to data segments. Examiner note: Hudgins in view of Mohebbi already taught corresponding of message queue, i.e.

claim's FIFO, to command data structure, see rationale of claim 17). It would have been obvious to one of ordinary skill in the art at the time of invention to adopt the teaching of Micalizzi in Mohebbi's system modified by Hudgins for the same reasons stated above.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mohebbi et al (US Pub. 2003/0108119) in view of Hudgins Jr. (US pat. 4615001, herein Hudgins) and in further view and Micalizzi Jr. et al (US Pat. 6434630, herein Micalizzi) and Fesas Jr. (US Pub. 2002/0009075, herein Fesas).

As in claim 21, Mohebbi, Hudgins and Micalizzi do not disclose the claim's four bytes. However, Fesas discloses wherein the command blocks further defined within the random access memory portions are each four bytes in length (pars. 10 and 33). It would have been obvious to one of ordinary skill in the art at the time of invention to include command block structure having length of four bytes as suggested by Fesas n Mohebbi's system modified by Hudgins and Micalizzi thus command blocks can be processed efficiently in four bytes unit and thereby further improve overall performance of the system (pars. 10 and 33, transferring interface for example of PDC four bytes packet).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this office action.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 36 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

When responding to the office action, Applicant is advised to provide the examiner with the paragraph numbers, and/or line numbers and page numbers in the application to assist examiner to locate the appropriate paragraphs.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

/Duc T Doan/

Patent Examiner